a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

A2 Cancel

22. (Amended Once) A circuit [is] in accordance with claim 16 wherein said first steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

New Claims:

Please add new claim 37-66 as follows:

37. (New) A system including a voice over IP telephone switch and at least one voice over IP telephone, the telephone including an apparatus for controlling the loop back of a differential mode signal received at the telephone on a first pair of conductors and transmitted from the telephone on a second pair of conductors, the apparatus comprising:

means for receiving the differential mode signal;

means for applying the differential mode signal to a first steering circuit and a second steering circuit;

A3 Cont.

means for generating a first signal to be transmitted on a first one of the second pair of conductors with said first steering circuit; and

means for generating a second signal to be transmitted on a second one of the second pair of conductors with said second steering circuit.

38. (New) A system in accordance with claim 37, wherein the apparatus further comprises:

means for transmitting said first and second signals on the second pair of conductors.

39. (New) A system in accordance with claim 38, wherein the apparatus further comprises:

means for receiving at the telephone a power signal; and

means for disabling at least one of said first steering circuit and said second steering circuit in response to receipt of said power signal.

40. (New) A system in accordance with claim 38, wherein the apparatus further comprises:

means for receiving at the telephone a power signal; and

means for distorting at least one of said first signal and said second signal in response to receipt of said power signal.

41. (New) A system in accordance with claim 38, wherein the apparatus further comprises:

A3 Cont.

means for mirroring current from at least one of said first steering circuit and said second steering circuit;

means for rectifying said mirrored current;

means for applying said rectified current to a voltage storage device;

means for using said voltage storage device to control at least one switch; and

means for disabling at least one of said first steering circuit and said second steering circuit with said at least one switch.

42. (New) A system in accordance with claim 38, wherein the apparatus further comprises:

means for mirroring current from at least one of said first steering circuit and said second steering circuit;

means for rectifying said mirrored current;

means for applying said rectified current to a voltage storage device;

means for using said voltage storage device to control at least one switch; and

means for distorting at least one of said first signal and said second signal with said at least one switch.

43. (New) A system including a voice over IP telephone switch and at least one voice over IP telephone, the voice over IP telephone device for receiving a differential mode signal on a first pair of conductors and transmitting a signal on a second pair of conductors, the device comprising:

a first steering circuit responsive to the differential mode signal on the first pair of conductors for generating a signal on one of the second pair of conductors; and

a second steering circuit responsive to the differential mode signal on the first pair of conductors for generating a signal on the other of the second pair of conductors.

A3 cont.

44. (New) A system in accordance with claim 43, wherein said device further comprises:

circuitry responsive to application of a DC voltage level disabling the first steering circuit.

45. (New) A system in accordance with claim 44, wherein said device further comprises:

circuitry responsive to application of said DC voltage level disabling the second steering circuit.

46. (New) A system in accordance with claim 43, wherein said device further comprises:

circuitry responsive to application of a DC voltage level distorting the differential mode signal prior to transmitting it on the second pair of conductors.

47. (New) A system in accordance with claim 43 wherein said first steering circuit comprises:

an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

48. (New) A system in accordance with claim 47 wherein said second steering circuit comprises an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

A3 Cont'

49. (New) A system in accordance with claim 48, wherein said device further comprises:

circuitry responsive to application of a DC voltage level disabling the first steering circuit.

50. (New) A system in accordance with claim 49, wherein said device further comprises:

circuitry responsive to application of said DC voltage level disabling the second steering circuit.

51. (New) A system in accordance with claim 48, wherein said device further comprises:

circuitry responsive to application of a DC voltage level distorting the differential mode signal prior to transmitting it on the second pair of conductors.

52. (New) A system in accordance with claim 43 wherein said first steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

53. (New) A system in accordance with claim 52 wherein said second steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

A3 Cont

54. (New) A system in accordance with claim 53, wherein said device further comprises:

circuitry responsive to application of a DC voltage level disabling the first steering circuit.

55. (New) A system in accordance with claim 54, wherein said device further comprises:

circuitry responsive to application of said DC voltage level disabling the second steering circuit.

56. (New) A system in accordance with claim 53, wherein said device further comprises:

circuitry responsive to application of a DC voltage level distorting the differential mode signal prior to transmitting it on the second pair of conductors.

57. (New) A system in accordance with claim 43, wherein said device further comprises:

a current mirror associated with said first steering circuit;

a voltage storage device coupled to said current mirror; and

a switch controlled by a voltage stored on said voltage storage device, said switch coupled to said second steering circuit for altering operation of said second steering circuit in response to the voltage stored on said voltage storage device.

58. (New) A system in accordance with claim 43, wherein said device further comprises:

A3 Cont

a current mirror associated with said first steering circuit;

a voltage storage device coupled to said current mirror; and

a switch controlled by a voltage stored on said voltage storage device, said switch coupled to said first steering circuit for altering operations of said first steering circuit in response to the voltage stored on said voltage storage device.

59. (New) A system in accordance with claim 57 wherein said first steering circuit comprises:

an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

60. (New) A system in accordance with claim 58 wherein said first steering circuit comprises:

an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

61. (New) A system in accordance with claim 59 wherein said second steering circuit comprises an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

62. (New) A system in accordance with claim 60 wherein said second steering circuit comprises an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

63. (New) A system in accordance with claim 57 wherein said first steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

64. (New) A system in accordance with claim 58 wherein said first steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

65. (New) A system in accordance with claim 63 wherein said second steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.